ABSTRACT

The present invention provides a method for parallel production of an MOS transistor in an MOS area of a substrate and a bipolar transistor in a bipolar area of the substrate. The method comprises generating an MOS preparation structure in the MOS area, wherein the MOS preparation structure comprises an area provided for a channel, a gate dielectric, a gate electrode layer and a mask layer on the gate electrode layer. Further, a bipolar preparation structure is generated in the bipolar area, which comprises a conductive layer and a mask layer on the conductive layer. For determining a gate electrode and a base terminal area, common structuring of the gate electrode layer and the conductive layer is performed. Further, the method comprises simultaneous generation of isolating spacing layers on side walls of the gate electrode layer in the MOS area and the conductive layer in the bipolar area by depositing a first and second spacing layer. In the MOS area, the isolating spacing layers serve for defining areas to be doped and in the bipolar area for the isolation of a base area and an emitter area. Subsequently, selective etching of the first spacing layer and the second spacing layer is performed in the MOS area and the bipolar area.

Figure 26